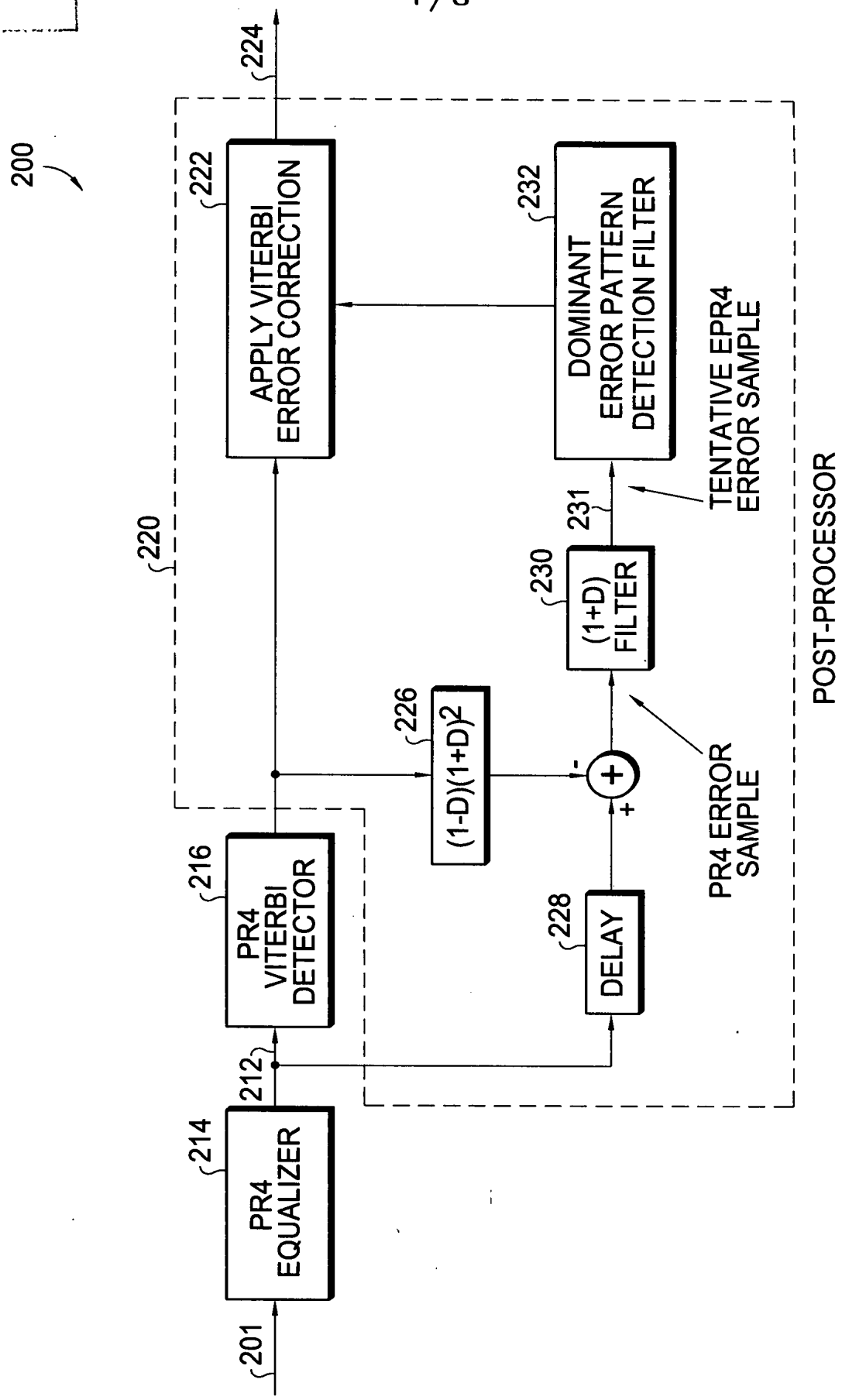


FIG. 1
PRIOR ART

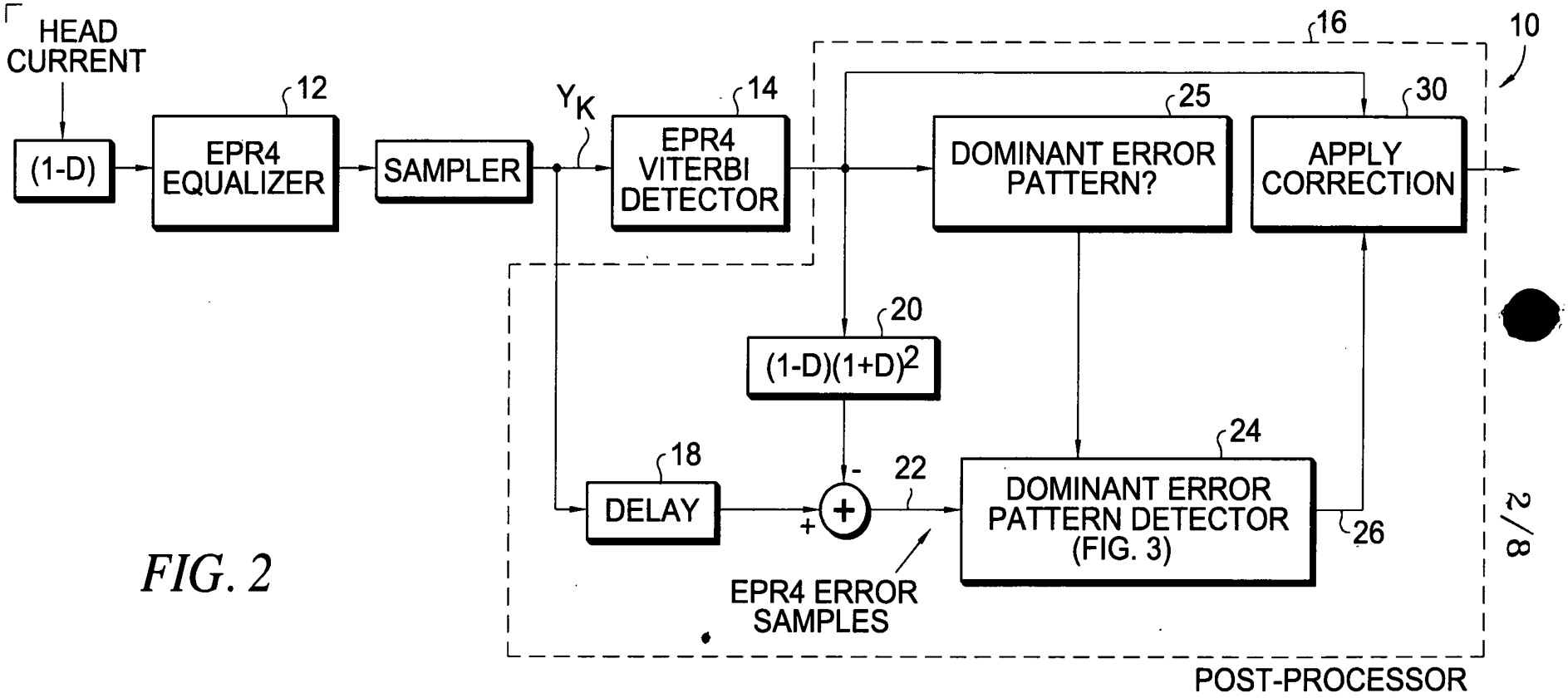


FIG. 2

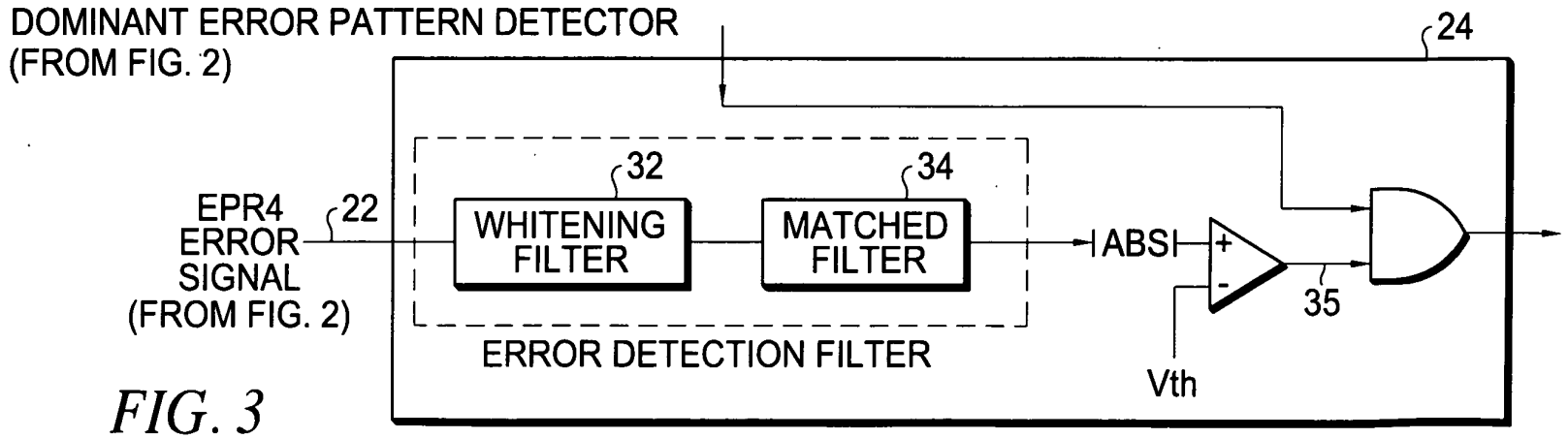


FIG. 3

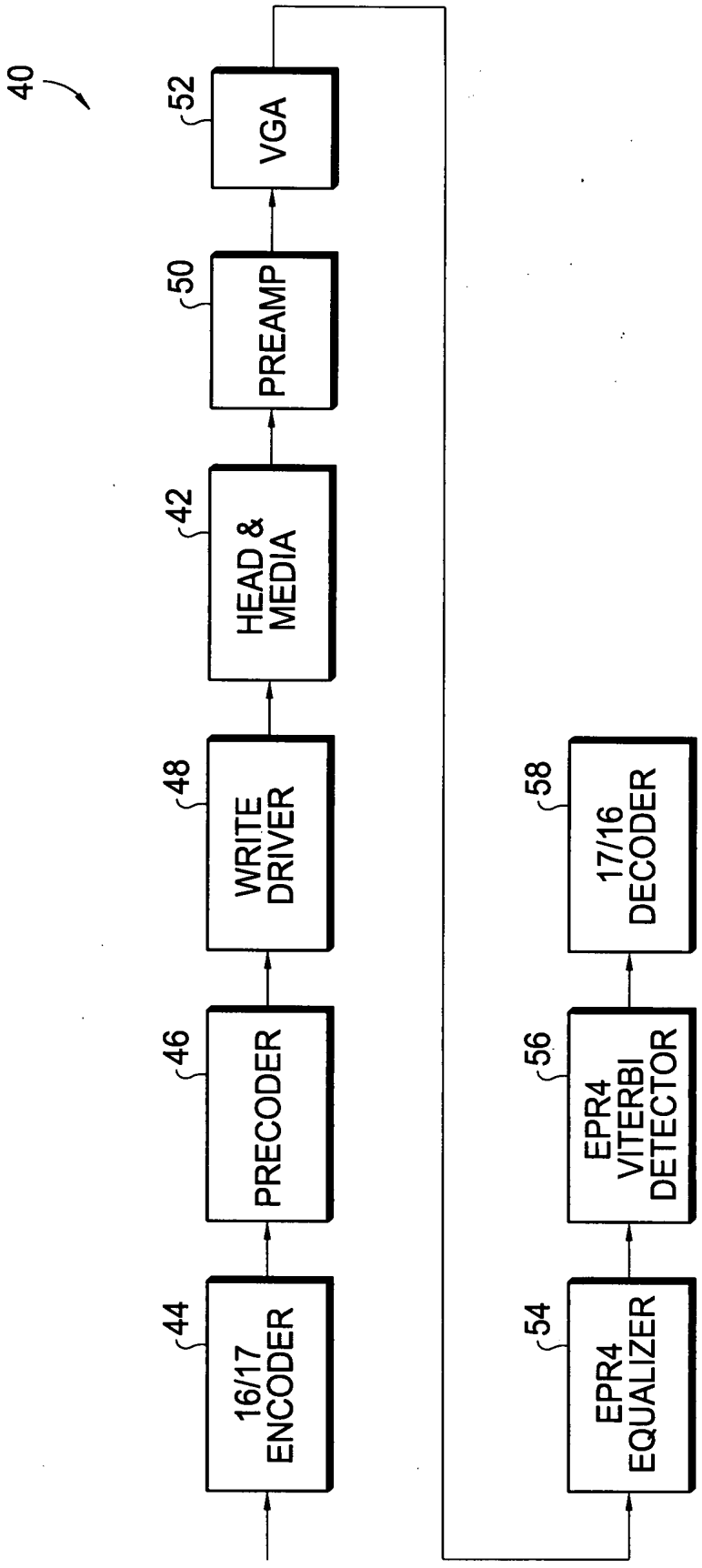
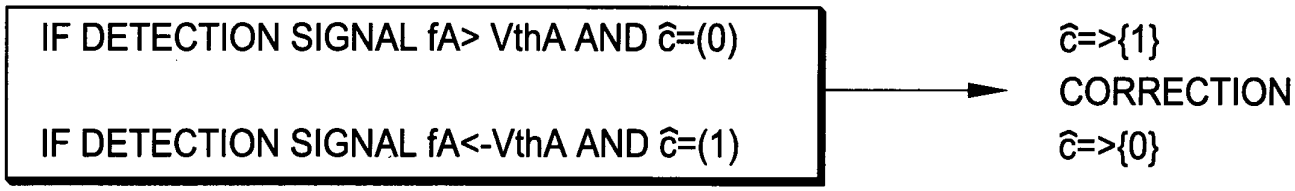

40
52
VGA
50
PREAMP
42
HEAD & MEDIA
48
WRITE DRIVER
46
PRECODER
44
16/17 ENCODER
54
EPR4 EQUALIZER
56
EPR4 VITERBI DETECTOR
58
17/16 DECODER

FIG. 4

ERROR EVENT A (ex={1} OR ex={-1})



ERROR EVENT B (ex={1,-1,1} OR ex={-1,1,-1})

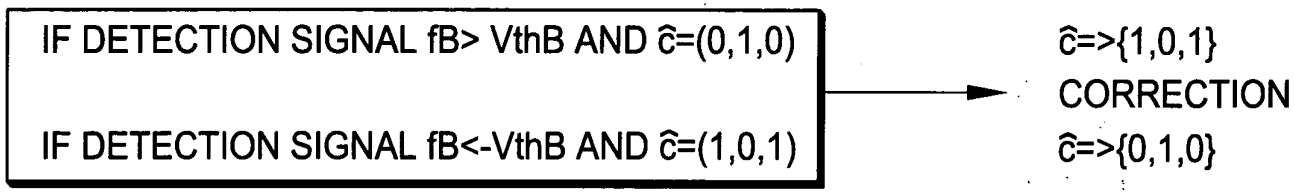


FIG. 5

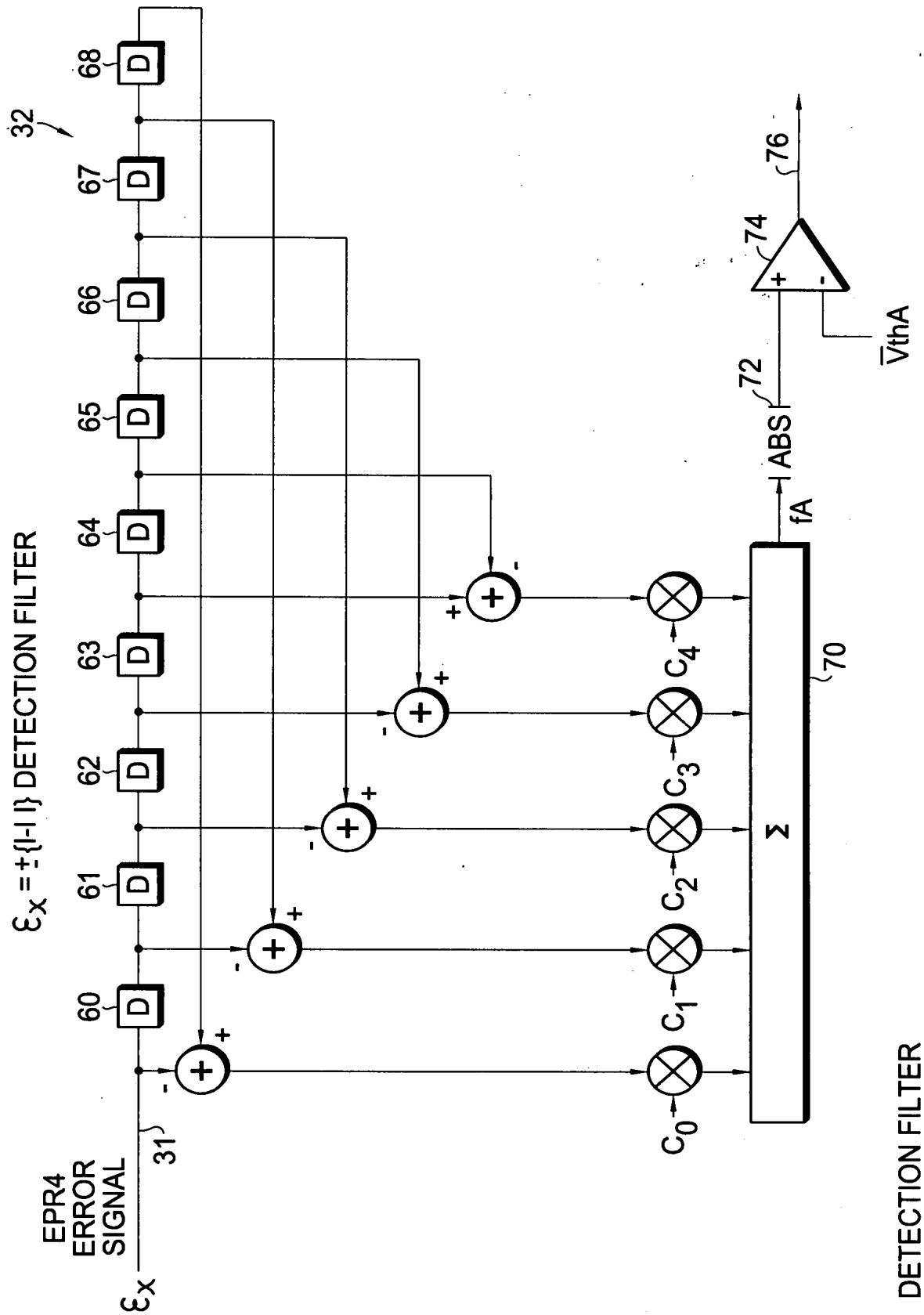

EPR4
ERROR
SIGNAL
ε_x
31
$\varepsilon_x = \pm\{I-I\}$ DETECTION FILTER
32
60
61
62
63
64
65
66
67
68
D
C_0
C_1
C_2
C_3
C_4
Σ
70
fA
ABS
72
74
76
$\overline{V}$thA
DETECTION FILTER
$fA=C_0(D^9-1)+C_1(D^8-D)+C_2(D^7-D^2)+C_3(D^6-D^3)-C_4(D^5-D^4)$

FIG. 6

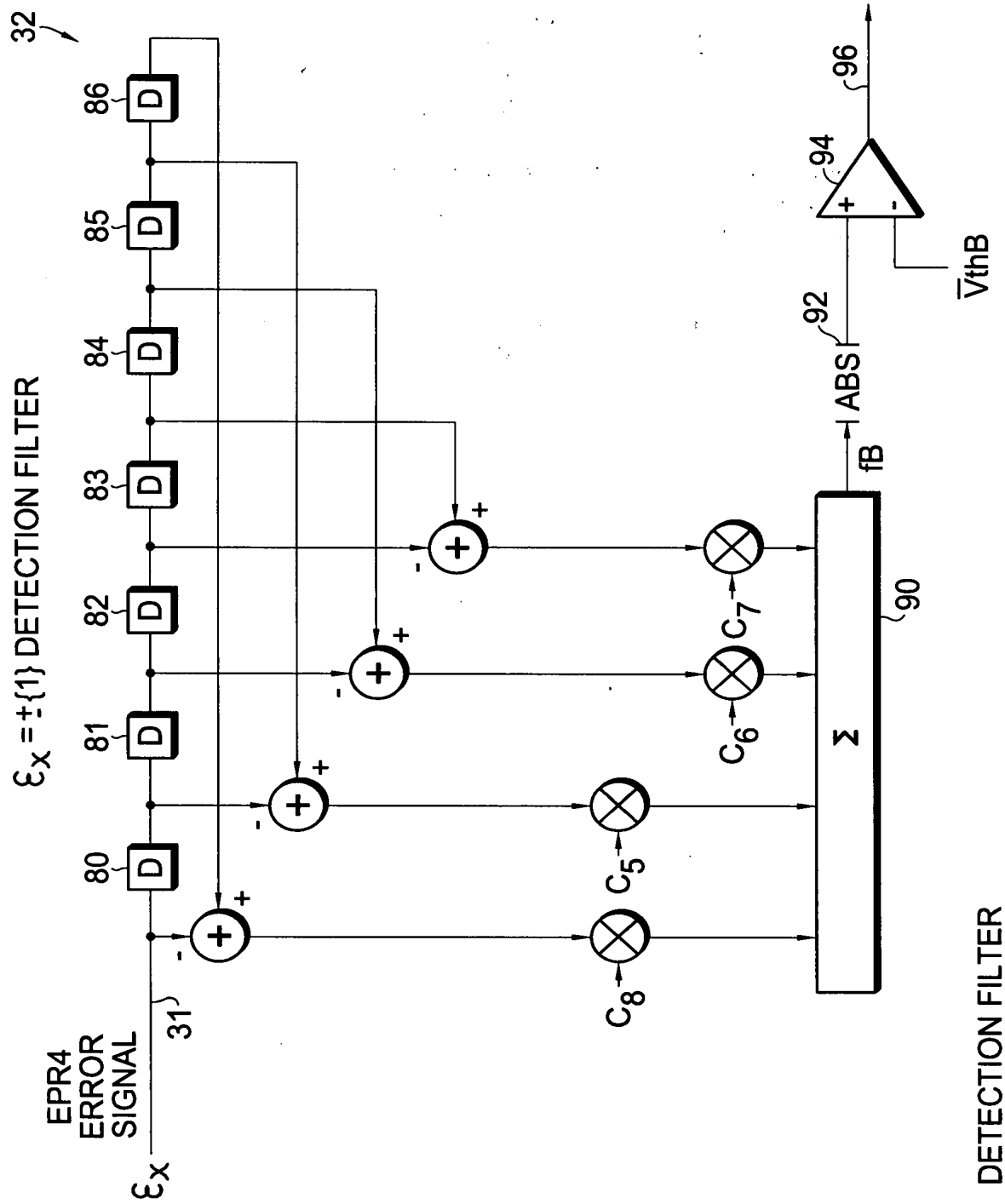

32
ε_X = ±{1} DETECTION FILTER
EPR4 ERROR SIGNAL
ε_X
31
80
81
82
83
84
85
86
D
C_8
C_5
C_6
C_7
Σ
90
fB
ABS
92
94
96
$\overline{V}$thB
DETECTION FILTER
$fB=C_8(D^7-1)+C_5(D^6-D)+C_6(D^5-D^2)+C_7(D^4-D^3)$

FIG. 7

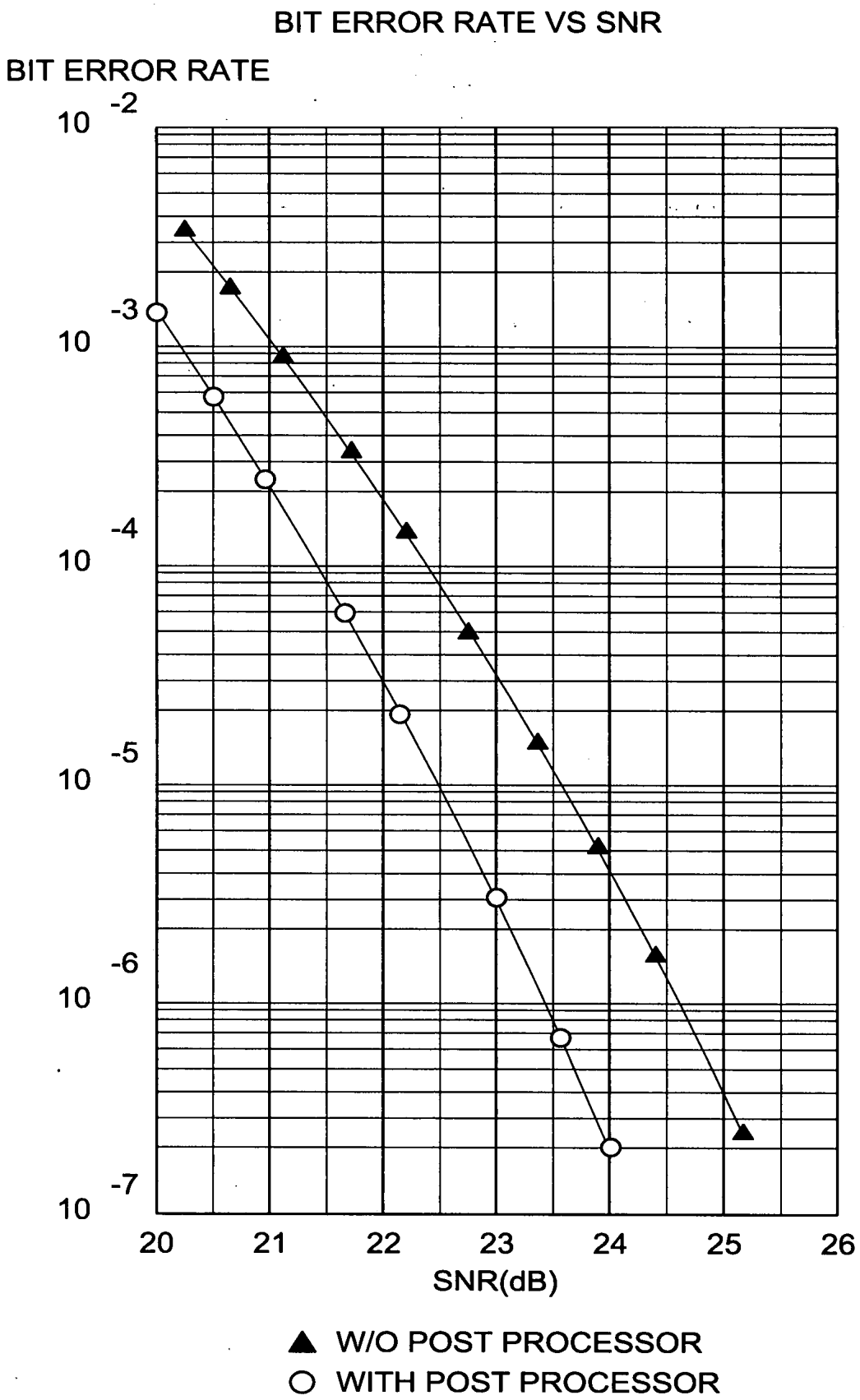

BIT ERROR RATE VS SNR
BIT ERROR RATE
10 -2
10 -3
10 -4
10 -5
10 -6
10 -7
20
21
22
23
24
25
26
SNR(dB)
W/O POST PROCESSOR
WITH POST PROCESSOR

FIG. 8

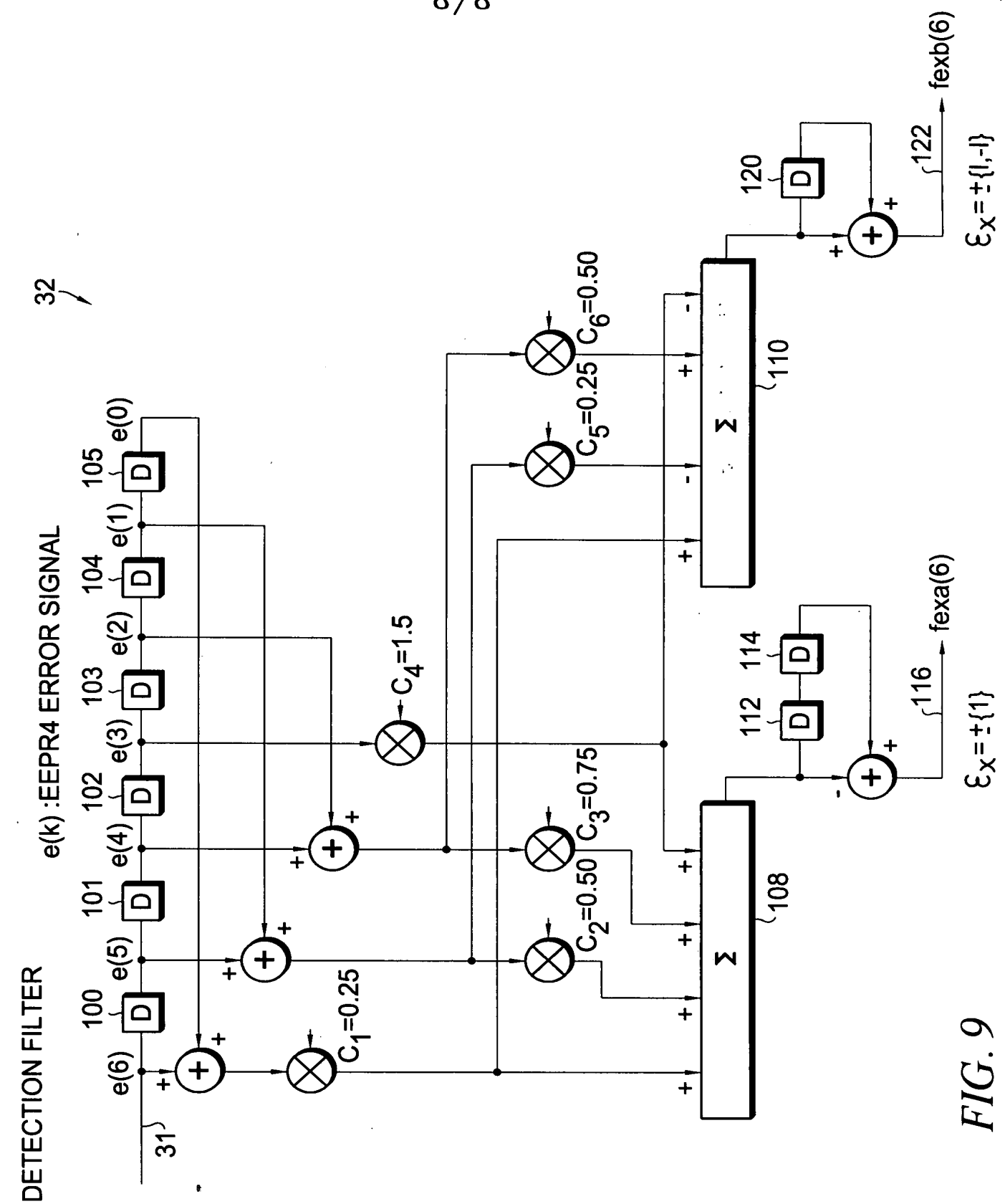

ERROR DETECTION FILTER
e(k) :EEPR4 ERROR SIGNAL
32
31
e(6)
e(5)
e(4)
e(3)
e(2)
e(1)
e(0)
100
101
102
103
104
105
D
C_1=0.25
C_2=0.50
C_3=0.75
C_4=1.5
C_5=0.25
C_6=0.50
Σ
108
110
112
114
116
120
122
fexa(6)
fexb(6)
ε_x=+{1}
ε_x=+{1,-1}

FIG. 9